(20 Marks)

c. Locality

d.

Standard cell

Full custom design.

USN

## Fourth Semester M.Tech. Degree Examination, June /July 2016 Advances in VLSI Design

Time: 3 hrs. Max. Marks: 100 Note: Answer any FIVE full questions. Explain CMOS inverter using transfer characteristic and describe aspect ratio with relevant 1 (10 Marks) Using switch logic, write CMOS NAND gate and CMOS NOR gate diagram. b. (06 Marks) Compare CMOS and BiCMOS technologies. (04 Marks) Explain MESFET under bias of V<sub>D</sub> below pinch off and bias at pinch off with its current – 2 a. voltage characteristic. (10 Marks) Derive an expression for the pinch-off voltage in MESFET with an active layer thickness of b. 't'. (06 Marks) Differentiate between MESFET and MODFET. c. (04 Marks) Describe the MIS system under three different biased conditions (i.e accumulation, depletion 3 and inversion region). b. Calculate the threshold voltage (V<sub>T</sub>) for a n-channel MIS device given the following  $N_a = 10^{17} \text{ cm}^{-3}$ ,  $Q_i = 10'' \text{ a/cm}^2$ , d = 20 nm and  $Q_{ms} = -0.95 \text{ V}$ . (08 Marks) With a neat diagram, explain two dimensional potential profile for a long channel MOSFET 4 device and short channel MOSFET device. (12 Marks) Describe the processing challenges to further CMOS miniaturization. b. (08 Marks) Explain the differences between bulk MOSFET and SOI MOSFET in the gate controlled 5 depletion region. (10 Marks) Discuss: b. i) Conventional Vs tactile computation ii) Molecular and biological computing. (10 Marks) Explain RC delay line using long silicon line using suitable mathematical analysis. 6 (10 Marks) b. What are super buffers? Explain inverting and non inverting nMOS super buffers. (10 Marks) Describe 4 input tally circuits. (10 Marks) Realize (AB + CD) = y in i) NMOS ii) CMOS technology, using static AOI. (05 Marks) Write a note on nMOS multiplxers. (05 Marks) 8 Discuss: a. Regularity b. Modularity

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